

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	1802	optimiz\$4 same mask\$4 same layer	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B
2	BRS	L2	182	(optimiz\$4 same mask\$4 same layer) and (data same structure)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B
3	BRS	L3	66	(optimiz\$4 same mask\$4 same layer) and (data same structure) and photolithograph\$4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B

	Type	L #	Hits	Search Text	DBs
4	BRS	L4	16	(optimiz\$4 same mask\$4 same layer) and (data same structure) and photolithograph\$4 and ("716"/\$.ccls. or "430"/\$.ccls.)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B
5	BRS	L5	116	(optimiz\$4 same mask\$4) and (data same layer) and (data same structure) and photolithograph\$4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B
6	BRS	L6	28	(optimiz\$4 same mask\$4) and (data same layer) and (data same structure) and photolithograph\$4 and ("716"/\$.ccls. or 430/4.ccls.)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B

	Type	L #	Hits	Search Text	DBs
7	BRS	L7	2	(optimiz\$4 same mask\$4) same (data same layer) same (data same structure) and photolithograph\$4 and ("716"/\$.ccls. or 430/4.ccls.)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B
8	BRS	L8	6	(optimiz\$4 same mask\$4) same (data same layer) same (data same structure) and photolithograph\$4	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TD B

	Document ID	Title	Current OR
1	US 20050044514 A1	Method and platform for integrated physical verifications and manufacturing enhancements	716/5
2	US 20050042527 A1	Phase shift mask including sub-resolution assist features for isolated spaces	430/5
3	US 20050014074 A1	GENERATING MASK PATTERNS FOR ALTERNATING PHASE-SHIFT MASK LITHOGRAPHY	430/5
4	US 20040230937 A1	Creating photolithographic masks	716/19
5	US 20040209176 A1	Model-based data conversion	430/5
6	US 20040191650 A1	Phase shift masking for complex patterns with proximity adjustments	430/5
7	US 20040181769 A1	System, apparatus and method for automated tapeout support	716/19
8	US 20040148584 A1	Mask pattern inspecting method, inspection apparatus, inspecting data used therein and inspecting data generating method	716/21
9	US 20030229879 A1	Model-based data conversion	716/19
10	US 20030013024 A1	Phase shift mask including sub-resolution assist features for isolated spaces	430/5
11	US 20030008222 A1	Phase shift mask layout process for patterns including intersecting line segments	430/5
12	US 20020100005 A1	Integrated verification and manufacturability tool	716/5
13	US 20020042007 A1	Fabrication method of semiconductor integrated circuit device	430/5
14	US 20010052107 A1	Integrated verification and manufacturability tool	716/4

	Document ID	Title	Current OR
15	US 6862725 B2	Method for manufacturing multi-kind and small quantity semiconductor products in a mass-production line and system thereof	716/19
16	US 6834375 B1	System and method for product yield prediction using a logic characterization vehicle	716/2
17	US 6795952 B1	System and method for product yield prediction using device and process neighborhood characterization vehicle	716/5
18	US 6785879 B2	Model-based data conversion	716/21
19	US 6777141 B2	Phase shift mask including sub-resolution assist features for isolated spaces	430/5
20	US 6733929 B2	Phase shift masking for complex patterns with proximity adjustments	430/5
21	US 6728946 B1	Method and apparatus for creating photolithographic masks	716/19
22	US 6664009 B2	Method and apparatus for allowing phase conflicts in phase shifting mask and chromeless phase edges	430/5
23	US 6654660 B1	Controlling thermal expansion of mask substrates by scatterometry	700/121
24	US 6566023 B2	Phase shifting circuit manufacture method and apparatus	430/5
25	US 6524752 B1	Phase shift masking for intersecting lines	430/5
26	US 6523165 B2	Alternating phase shift mask design conflict resolution	716/21
27	US 6415421 B1	Integrated verification and manufacturability tool	716/4

	Document ID	Title	Current OR
28	US 5689432 A	Integrated circuit design and manufacturing method and an apparatus for designing an integrated circuit in accordance with the method	716/18